

REMARKS

Claims 7-12 are pending in the application. Applicant respectfully requests reconsideration in view of the Remarks.

Claims 7-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kunii, et al. (JP 5-275701). In addition, Claims 7-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nakamura et al. (JP 5-206165) ("Nakamura"). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 SPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the * * * claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner states that Kunii discloses in Figure 8, a thin film transistor comprising a semiconductor film 2 or poly-silicon film (as in claim 9), a first gate insulating film 9 or silicon oxide film (as in claim 8), a second gate insulating film 8 and a gate electrode 7 formed on one major surface of a substrate 1. The Examiner also asserts that the first gate insulating film covers the one major surface of the substrate of the semiconductor film other than a contact region. Applicant respectfully traverses.

Claim 7 includes the following limitation: "wherein said first gate insulating film covers said one major surface of the substrate and all regions of said semiconductor film other than a contact region." Accordingly, in the structure of claim 7, a first gate insulating film covering a semiconductor film is not only formed on the semiconductor film, but is also formed on a first major surface of a substrate. Kunii does not disclose, teach, or suggest that limitation.

As shown in Figure 8 of Kunii, the first gate insulating film 9 is not formed to cover the one major surface of the substrate and all regions of the semiconductor film other than a contact region. Instead, Figure 8 discloses that the gate insulating film 9 covers only the semiconductor film 2. Figure 8 does not disclose that the first gate insulating film covers the major surface of the substrate. At best, only an end portion of the gate insulating film touches a portion of the substrate.

The Examiner also states that Nakamura discloses in Figures 1-4, a thin film transistor comprising a semiconductor film 2 or poly-silicon film (as in claim 9), a first gate insulating film 9 or silicon oxide film (as in claim 8), a second gate insulating film 8 and a gate electrode 4 formed on one major surface of a substrate 1. The Examiner also asserts that the first gate insulating film covers the one major surface of the substrate of the semiconductor film other than a contact region. Applicant respectfully traverses.

As stated above, claim 7 includes the following limitation: "wherein said first gate insulating film covers said one major surface of the substrate and all regions of said semiconductor film other than a contact region." Nakamura does not disclose that the first gate insulating film covers the one major surface of the substrate other than a contact region. Instead, Nakamura discloses that the gate insulating film does not cover the substrate at all. The gate insulating film of Nakamura only covers a semiconductor film at the contact region.

Accordingly, Kunii and Nakamura do not anticipate claim 7. In addition, because claims 8-9 include all of the limitations of claim 7, Kunii and Nakamura do not anticipate claims 8-9. For at least the foregoing reasons, the anticipation rejection of claims 7-9 based on both Kunii and Nakamura is improper. Applicant respectfully requests that both rejections under 35 U.S.C. § 102(b) be withdrawn.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kunii (U.S. 5,412,493) in view of Codama (U.S. 5,292,675). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

Claim 10 claims a two-layer gate insulating film with the second gate insulating film including the following limitation: "said second gate insulating film is made of a material for supplying hydrogen to said semiconductor film and has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode." The

Examiner asserts Kunii discloses a thin film transistor comprising a semiconductor film or poly-silicon film (as in claim 12), a first gate insulating film 7 or silicon oxide film (as in claim 11), a second gate insulating film 8 and a gate electrode 9 formed on a surface of substrate 1, and that the first gate insulating film covers the semiconductor film and the second gate insulating film is made of a material or silicon nitride film (as in claim 11) for supplying hydrogen to the semiconductor film. The Examiner cites Codama for the teaching that Codama discloses a gate insulating film 7 with a smaller film thickness in a region not covered with a gate electrode 8 than gate insulating film 9 in a region covered with said gate electrode. The Examiner points to Figure 1 and col. 4, lines 26-68 of Codama for support. Applicant respectfully traverses.

The Examiner attempts to combine Kunii, which has the two layered gate insulating film, with Codama, which only has the single layer gate insulating film, to obtain all of the limitations of claim 10. An Examiner cannot establish obviousness by locating references that describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would have impelled one skilled in the art to do what the patent applicant has done. *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. Int. 1993). The references, when viewed by themselves and not in retrospect, must suggest the invention. *In Re Skoll*, 187 U.S.P.Q. 481 (C.C.P.A. 1975).

Neither Kunii nor Codama provide the motivation to combine the two references to reach the claimed invention. In fact, the disclosure in Kunii specifically discusses the advantages of using a two-layer gate insulating film over a single gate insulating film. See col. 7 line 67 to col. 8, line 11. Accordingly, with that teaching, one skilled in the art would not look to a single gate insulating film to improve upon the two-layer gate insulating film of Kunii.

In addition, claim 10 claims that the **second** gate insulating film that has a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode. There is nothing in Codama that would suggest that the gate insulating film could be utilized as a second gate insulating film. Thus, there is no motivation to combine the single layer structure gate of Codama with Kunii.

Moreover, both the suggestion and the expectation of success are found in Applicant's disclosure. According to the present invention, both a first gate insulating film and a second gate

insulating film are present at least over the entire region where the semiconductor film is formed. With such a structure, it is possible to simultaneously achieve a number of advantages such as the second gate insulating film (i) allowing for sufficient hydrogen supplying capability and (ii) blocking intrusion of contamination materials from the substrate or from the upper layers into the semiconductor film, and the first gate insulating film, and (iii) maintaining better conformity with respect to the semiconductor film to prevent introduction of defects into the semiconductor film due to interlayer nonconformity. By covering the entire semiconductor film by a gate insulating film of a multi-layer structure, these functionalities can be achieved to a satisfactory degree. Kunii and Codama do not teach or suggest the combination of advantages that are achieved by the claimed invention.

Applicant further maintains that the Examiner has used an improper standard in arriving at the rejection of the above claims. In applying Section 103, the U.S. Court of Appeals for the Federal Circuit has consistently held that one must consider both the invention and the prior art "as a whole," not from improper hindsight gained from consideration of the claimed invention. See *Interconnect Planning Corp. v. Feil*, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985) and cases cited therein. According to the *Interconnect* court

"[n]ot only must the claimed invention as a whole be evaluated, but so also must the references as a whole, so that their teachings are applied in the context of their significance to a technician at the time - a technician without our knowledge of the solution." *Id.*

In this case, the Examiner states that the single layer gate insulating film can be combined with a two-layer gate insulating film, but does not point to any reference that provides the teaching as to that relationship. Applicant submits that when Kunii and Codama are applied in context, a person skilled in the art would not arrive at Applicant's claimed limitations. Thus, claims 10-12 are patentable over Kunii and Codama. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura in view of Codama. As with the Kunii reference, the Examiner attempts to combine Nakamura, which has the two layered gate insulating film, with Codama, which only has the single layer gate insulating film, to obtain all of the limitations of claim 10. Accordingly, all of the

arguments set forth above, apply to the combination of the Nakamura reference combined with Codama. Moreover, there is nothing in Nakamura that would suggest looking to a single layer gate insulating film. Thus, claims 10-12 are patentable over Nakamura and Codama. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned. In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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